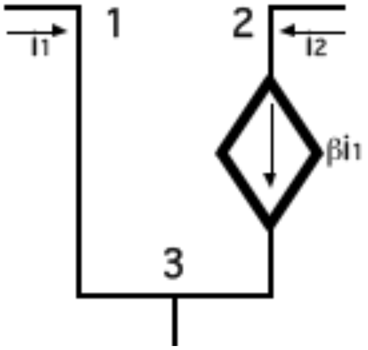
TRANSISTORS

Transistor – a three-terminal device for which the voltage or current at one terminal controls the electrical behavior of the other terminals.

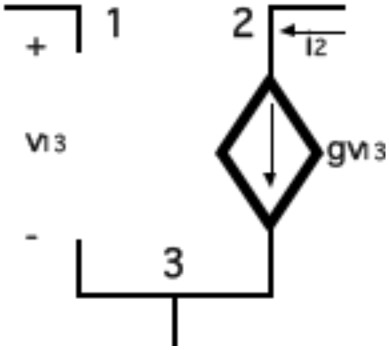
Bipolar Junction Transistor (BJT) – a three-terminal device for which the current at one terminal controls the electrical behavior of the other terminals.



Current-Controlled (Dependent) Current Source

$i_2 = \beta\, i_1$

Field Effect Transistor (FET) – a three-terminal device for which a voltage related to one terminal controls the electrical behavior of the other terminals.



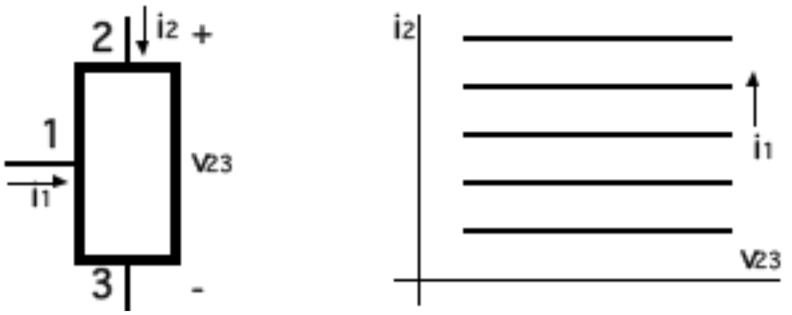
Voltage-Controlled (Dependent) Current Source

$i_2 = g\, v_{13}$

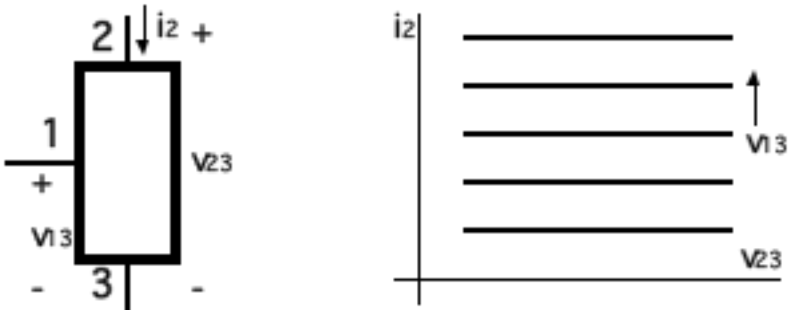
TRANSISTOR IV CHARACTERISTICS

IV Characteristic – the current-voltage behavior of a transistor is often represented as a set of curves, each of which corresponds to a different control current or voltage. The desired operation is limited to specific ranges of current and voltage, e.g. active regions. The nonlinear device must be biased to the desired operating point by an external circuit.

Examples:



$i_2 = \beta\, i_1$



$i_2 = g\, v_{13}$

Typical Applications

- Signal Amplification – a small signal is replicated and amplified
- Switching – a low-power input controls a high power output
- Logic Operations – a digital logic function is implemented

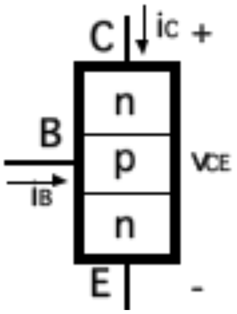
Transistors may be implemented in semiconductors as discrete devices or as integrated circuits.

BIPOLAR JUNCTION TRANSISTOR

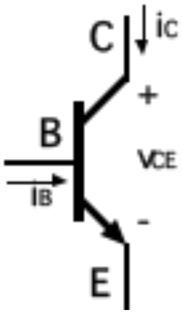
Bipolar Junction Transistor (BJT) – device formed by a p-type material between two n-type materials or an n-type material between two p-type materials.

Terminal Nomenclature
Base (B), Collector (C), and Emitter (E)

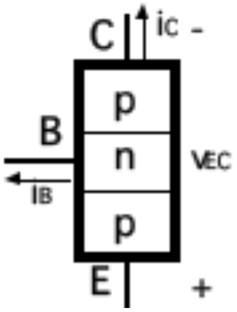
npn BJT: Structure



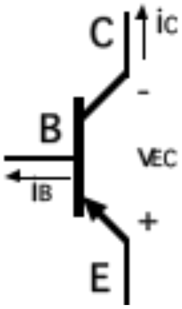
Circuit Symbol



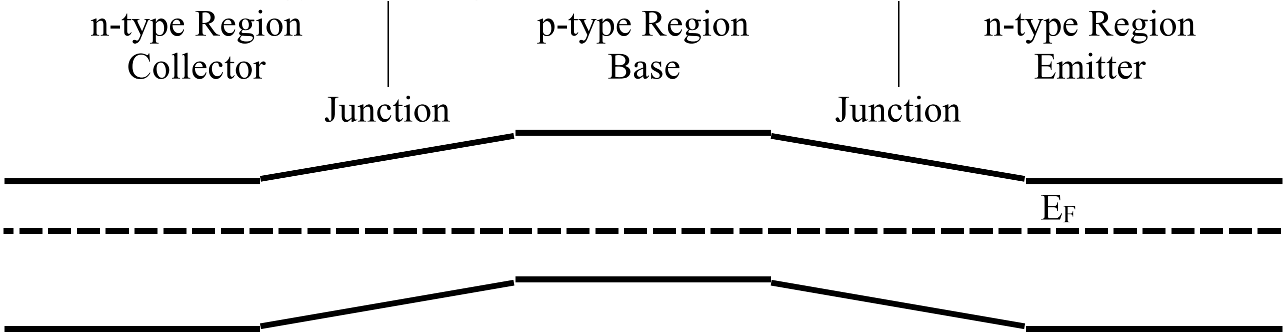
pnp BJT: Structure



Circuit Symbol



Equilibrium Energy Band Diagram for npn Structure

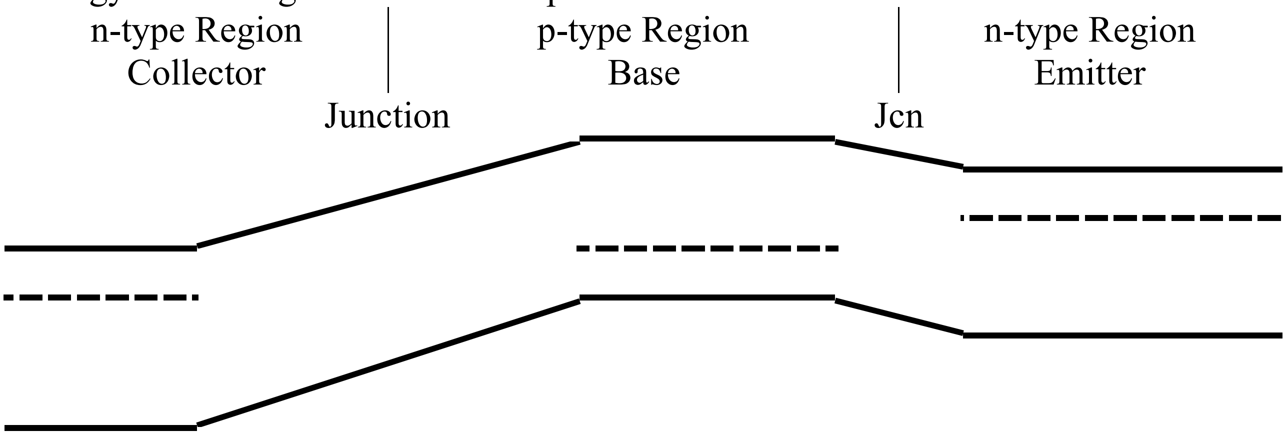


BJT OPERATING CONDITIONS

BJT Operating Conditions

- Base-Emitter Junction – Forward Bias
- Collector-Base Junction – Reverse Bias

Energy Band Diagram for Biased npn Structure



Base-Emitter Junction under Forward Bias

- Junction width narrows
- Diffusion current dominates
- Holes injected into the emitter region
- Electrons injected (emitted) into the base region

Base-Collector Junction under Reverse Bias

- Junction width broadens
- Drift current dominates
- Holes extracted from collector region near the junction
- Electrons extracted (collected) from base region near the junction

Desired Operation

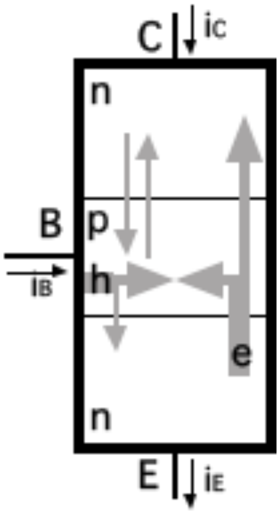
Electrons injected from the emitter into the base diffuse across the undepleted base region and are captured by the high electric field in the base-collector junction. Electrons lost to recombination in the base region do not contribute to the collector current.

The design depends on the width of the base region, a diffusion coefficient for electrons, and the average recombination lifetime for electrons.

BJT CURRENTS

BJT Currents – a summary of important currents in an npn transistor is shown below. (Some secondary effects are omitted.)

- Emitter electron current i_{En} and hole current i_{Ep}
- Collector current $i_C \sim i_{Cn}$
- Base current $i_B \sim i_{Bp}$
- Reverse-bias thermally-generated emitter-base current (neglected in further analysis)



The emitter injection efficiency $\gamma = i_{En}/(i_{En} + i_{Ep})$

The base transport factor $\alpha_F = i_{Cn}/i_{En}$

Then, the current transfer ratio

$$\alpha_o = i_C/i_E \sim (i_{Cn}/i_E) = (i_{Cn}/i_{En})\,[i_{En}/(i_{En} + i_{Ep})] = \alpha_F\,\gamma$$

Kirchhoff's Current Law for the transistor gives

$$+ i_C + i_B - i_E = 0 \quad \text{or} \quad + i_B = + i_E - i_C$$

Hence, the gain is

$$\beta = i_C/i_B = i_C/(i_E - i_C) = (i_C/i_E)/[1 - (i_C/i_E)] = (\alpha_o)/[1 - (\alpha_o)]$$

To produce a large gain β, the current transfer ratio α_o (and the base transport factor α_F and the emitter injection efficiency γ) must be near unity.

Design optimization

- Highly doped emitter (n+): $i_E \sim i_{En}$ and $\gamma = i_{En}/(i_{En} + i_{Ep})$ is near unity
- Narrow base width and light base doping: little recombination in the base region (i.e. α_F is near unity)

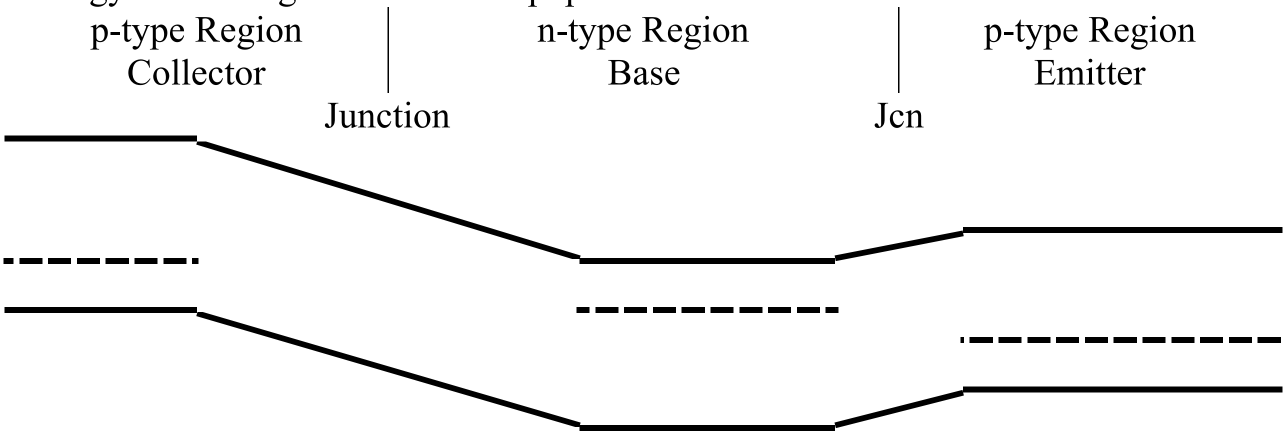
Note that the emitter and collector are typically doped differently.

BJT OPERATING CONDITIONS

BJT Operating Conditions

- Base-Emitter Junction – Forward Bias
- Collector-Base Junction – Reverse Bias

Energy Band Diagram for Biased pnp Structure



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BJT CURRENTS

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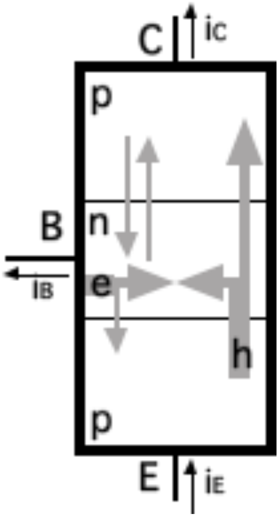


The emitter injection efficiency $\gamma = i_{Ep}/(i_{En} + i_{Ep})$

The base transport factor $\alpha_F = i_{Cp}/i_{Ep}$

Then, the current transfer ratio

$$\alpha_o = i_C/i_E \sim (i_{Cp}/i_E) = (i_{Cp}/i_{Ep})\,[i_{Ep}/(i_{En} + i_{Ep})] = \alpha_F\, \gamma$$

Kirchhoff's Current Law for the transistor gives

$$+ i_C + i_B - i_E = 0 \quad \text{or} \quad + i_B = + i_E - i_C$$

Hence, the gain is

$$\beta = i_C/i_B = i_C/(i_E - i_C) = (i_C/i_E)/[1 - (i_C/i_E)] = (\alpha_o)/[1 - (\alpha_o)]$$

To produce a large gain β, the current transfer ratio α_o (and the base transport factor α_F and the emitter injection efficiency γ) must be near unity.

Design optimization

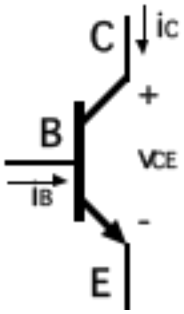
- Highly doped emitter (p+): $i_E \sim i_{Ep}$ and $\gamma = i_{Ep}/(i_{En} + i_{Ep})$ is near unity
- Narrow base width and light base doping: little recombination in the base region (i.e. α_F is near unity)

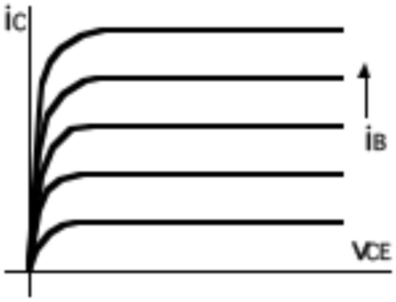
Note that the emitter and collector are typically doped differently.

SUMMARY OF BJT BEHAVIOR

The bipolar junction transistor current amplification with gain $\beta = i_C/i_B$.

npn BJT

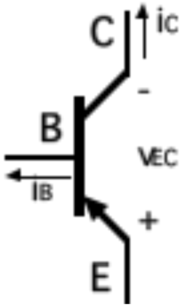


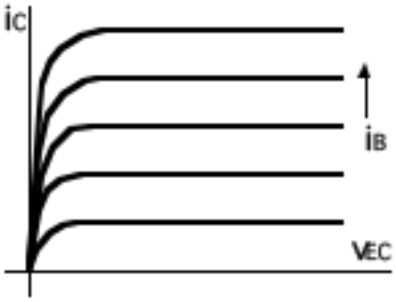


npn BJT Operating Conditions

- Forward Bias of Base-Emitter Junction v_{BE} > turn-on voltage
- Reverse Bias of Collector-Base Junction $v_{BC} < 0$ or $v_{CB} > 0$

pnp BJT





pnp BJT Operating Conditions

- Forward Bias of Base-Emitter Junction v_{EB} > turn-on voltage
- Reverse Bias of Collector-Base Junction $v_{CB} < 0$ or $v_{BC} > 0$

Regions in the Common-Emitter IV Characteristic

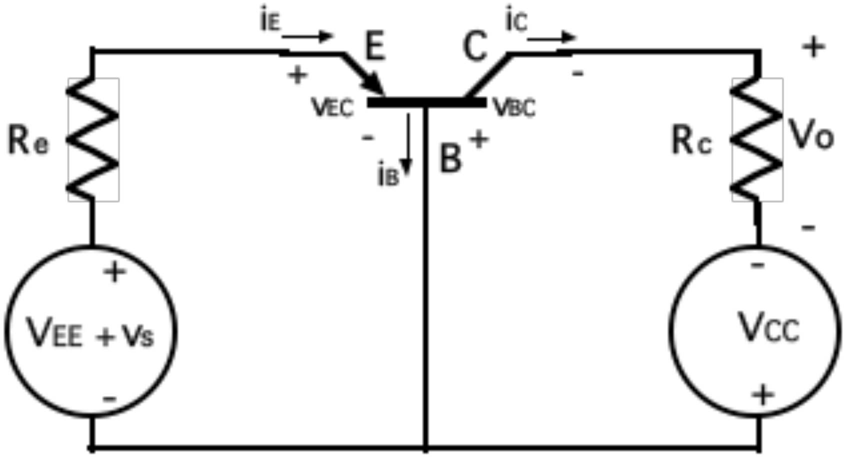
- Saturation – the base-collector junction is not reverse biased for low values of v_{CE} (npn) or v_{EC} (pnp) and i_C is not proportional to i_B.
- Active – the normal operating region in which $i_C = \beta i_B$.
- Breakdown (not shown) – the active region limit for large values of v_{CE} (npn) or v_{EC} (pnp) when breakdown occurs in the collector-base junction

Other secondary effects may be considered for more accurate representations, but these effects are beyond the scope of this class.

COMMON-BASE BJT CIRCUIT AND ANALYSIS

Common-Base Biasing Circuit with a pnp BJT

- Forward Bias of Base-Emitter Junction v_{EB} > turn-on voltage
- Reverse Bias of Collector-Base Junction $v_{CB} < 0$ or $v_{BC} > 0$



Analysis for Operating Point (v_{BC},i_C) with $v_S = 0$.

Kirchhoff's-Voltage-Law on Emitter Side ($v_{EC} = V_{to}$):

$$- V_{EE} + i_E R_e + V_{to} = 0 \quad \text{or} \quad i_E = (1/R_e)(V_{EE} - V_{to})$$

and

$$i_C = \alpha_o i_E = (\alpha_o/R_e)(V_{EE} - V_{to})$$

Kirchhoff's-Voltage-Law on Collector Side (the Load-Line Equation):

$$- V_{CC} + i_C R_c + v_{BC} = 0 \quad \text{or} \quad v_{BC} = V_{CC} - i_C R_c$$

With no signal $v_S = 0$

$$V_o = i_C R_c = (\alpha_o R_c/R_e)(V_{EE} - V_{to})$$

With a signal v_S

$$V_o = i_C R_c = (\alpha_o R_c/R_e)(V_{EE} - V_{to}) + (\alpha_o R_c/R_e)(v_S)$$

Graphical Analysis

Load-Line

$$- V_{CC} + i_C R_c + v_{BC} = 0$$

Intercepts

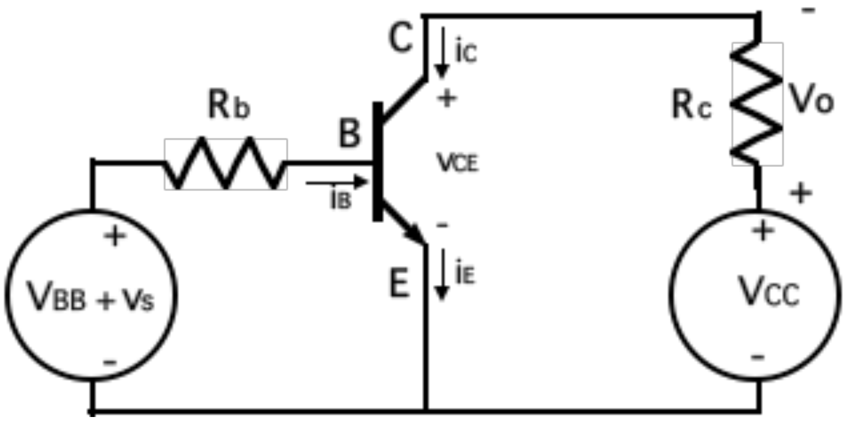
$v_{BC} = V_{CC}$

$i_C = V_{CC}/R_c$

COMMON-EMITTER BJT AMPLIFIER AND ANALYSIS

Common-Emitter Biasing Circuit with an npn BJT

- Forward Bias of Base-Emitter Junction v_{BE} > turn-on voltage
- Reverse Bias of Collector-Base Junction $v_{BC} < 0$ or $v_{CB} > 0$



Analysis for Operating Point (v_{CE},i_C) with $v_S = 0$.

Kirchhoff's-Voltage-Law on Base Side ($v_{BE} = V_{to}$):

$$- V_{BB} + i_B R_b + V_{to} = 0 \quad \text{or} \quad i_B = (1/R_b)(V_{BB} - V_{to})$$

and

$$i_C = \beta i_B = (\beta/R_b)(V_{BB} - V_{to})$$

Kirchhoff's-Voltage-Law on Collector Side (the Load-Line Equation):

$$- V_{CC} + i_C R_c + v_{CE} = 0 \quad \text{or} \quad v_{CE} = V_{CC} - i_C R_c$$

With no signal $v_S = 0$

$$V_o = i_C R_c = (\beta R_c/R_b)(V_{BB} - V_{to})$$

With a signal v_S

$$V_o = i_C R_c = (\beta R_c/R_b)(V_{BB} - V_{to}) + (\beta R_c/R_b)(v_S)$$

Graphical Analysis

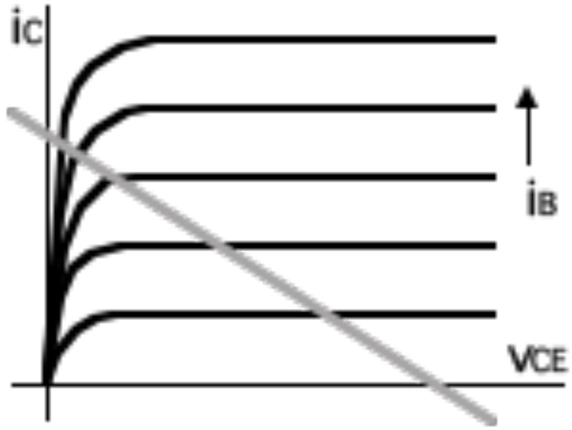
Load-Line

$$- V_{CC} + i_C R_c + v_{CE} = 0$$

Intercepts

$v_{CE} = V_{CC}$

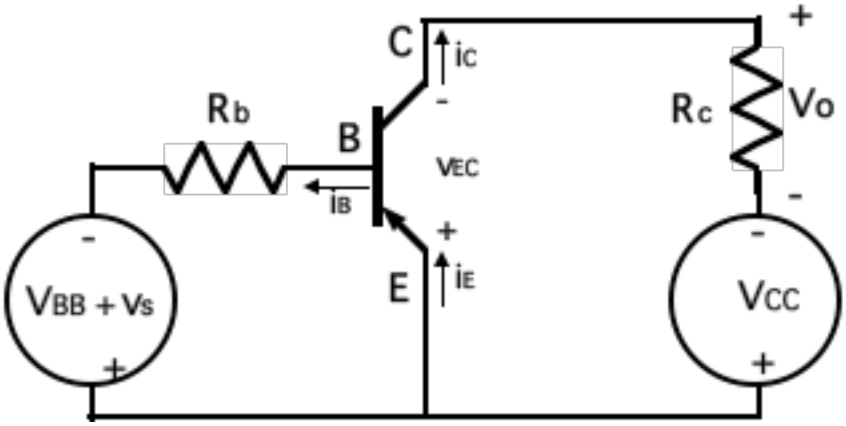
$i_C = V_{CC}/R_c$



COMMON-EMITTER BJT AMPLIFIER AND ANALYSIS

Common-Emitter Biasing Circuit with a pnp BJT

- Forward Bias of Base-Emitter Junction v_{EB} > turn-on voltage
- Reverse Bias of Collector-Base Junction $v_{CB} < 0$ or $v_{BC} > 0$



Analysis for Operating Point (v_{EC},i_C) with $v_S = 0$.

Kirchhoff's-Voltage-Law on Base Side ($v_{EB} = V_{to}$):

$$- V_{BB} + i_B R_b + V_{to} = 0 \quad \text{or} \quad i_B = (1/R_b)(V_{BB} - V_{to})$$

and

$$i_C = \beta i_B = (\beta/R_b)(V_{BB} - V_{to})$$

Kirchhoff's-Voltage-Law on Collector Side (the Load-Line Equation):

$$- V_{CC} + i_C R_c + v_{EC} = 0 \quad \text{or} \quad v_{EC} = V_{CC} - i_C R_c$$

With no signal $v_S = 0$

$$V_o = i_C R_c = (\beta R_c/R_b)(V_{BB} - V_{to})$$

With a signal v_S

$$V_o = i_C R_c = (\beta R_c/R_b)(V_{BB} - V_{to}) + (\beta R_c/R_b)(v_S)$$

Graphical Analysis

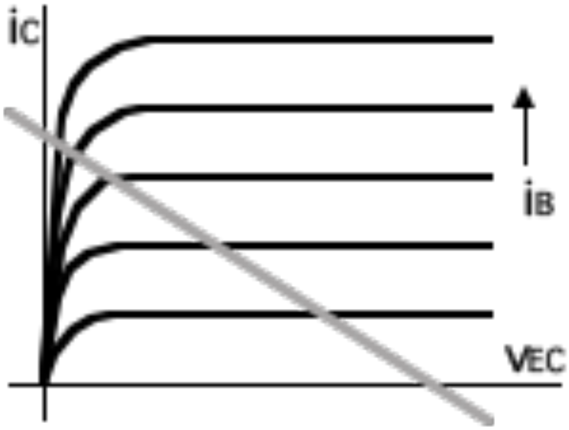
Load-Line

$$- V_{CC} + i_C R_c + v_{EC} = 0$$

Intercepts

$v_{EC} = V_{CC}$

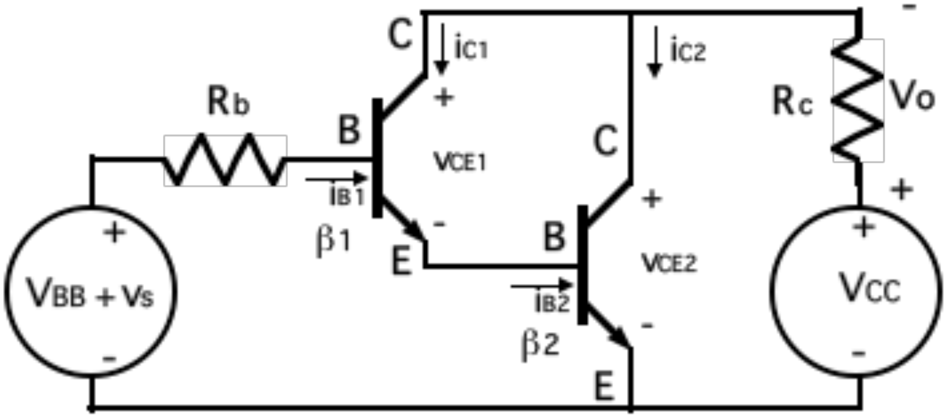
$i_C = V_{CC}/R_c$



DARLINGTON AMPLIFIER AND ANALYSIS

Common-Emitter Biasing Circuit with dual-npn BJT's

- Forward Bias of Base-Emitter Junctions v_{BE} > turn-on voltage
- Reverse Bias of Collector-Base Junctions $v_{BC} < 0$ or $v_{CB} > 0$



Kirchhoff's-Voltage-Law on Base Side ($v_{BE1} = v_{BE2} = V_{to}$):

$$-(V_{BB} + v_S) + i_{B1} R_b + 2V_{to} = 0 \quad \text{or} \quad i_{B1} = (1/R_b)[(V_{BB} + v_S) - 2V_{to}]$$

and

$$i_{C1} = \beta_1 i_{B1} = (\beta_1/R_b)[(V_{BB} + v_S) - 2V_{to}]$$

Also, noting that $\beta_1/\alpha_{o1} = 1 + \beta_1$

$$i_{C2} = \beta_2 i_{B2} = \beta_2 i_{E1} = \beta_2 i_{C1}/\alpha_{o1} = \beta_2\beta_1 i_{B1}/\alpha_{o1} = \beta_2(1 + \beta_1)i_{B1}$$

$$i_{C2} = \beta_2(1 + \beta_1)(1/R_b)[(V_{BB} + v_S) - 2V_{to}]$$

Then,

$$i_{C1} + i_{C2} = [\beta_1 + \beta_2(1 + \beta_1)]\{(1/R_b)[(V_{BB} + v_S) - 2V_{to}]\}$$

$$i_{C1} + i_{C2} = [\beta_1 + \beta_2 + \beta_1\beta_2]\{(1/R_b)[(V_{BB} + v_S) - 2V_{to}]\}$$

The output voltage is

$$V_o = (i_{C1} + i_{C2})R_c = [\beta_1 + \beta_2 + \beta_1\beta_2]\{(R_c/R_b)[(V_{BB} + v_S) - 2V_{to}]\}$$

Note that the overall gain of the dual-transistor configuration is

$$\beta_{Dual} = (i_{C1} + i_{C2})/i_{B1} = (\beta_1 + \beta_2 + \beta_1\beta_2)$$

If the transistors are identical with a large gain ($\beta_1 = \beta_2 = \beta >> 1$),

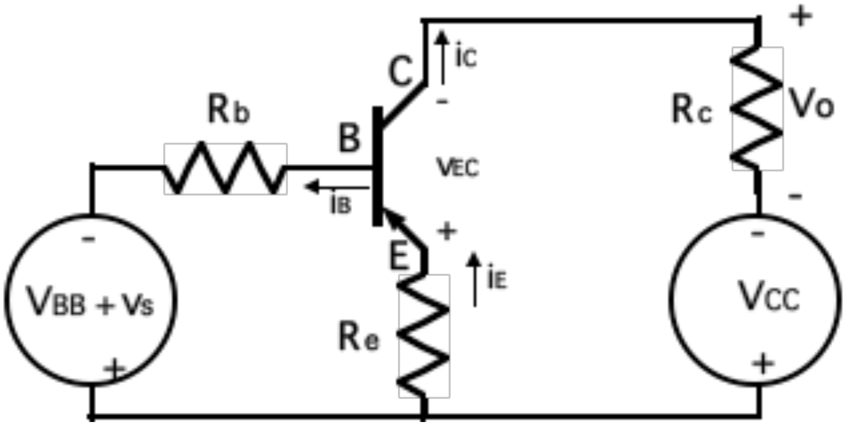
$$\beta_{Dual} = (i_{C1} + i_{C2})/i_{B1} = \beta(2 + \beta) \sim \beta^2$$

The overall gain can be increased further with additional transistors.

COMMON-EMITTER BJT AMPLIFIER VARIATION

Common-Emitter Biasing Circuit with a pnp BJT

- Forward Bias of Base-Emitter Junction v_{EB} > turn-on voltage
- Reverse Bias of Collector-Base Junction $v_{CB} < 0$ or $v_{BC} > 0$



Analysis for Operating Point (v_{EC},i_C) with $v_S = 0$.

Kirchhoff's-Voltage-Law on Base Side ($v_{EB} = V_{to}$):

$$- V_{BB} + i_B R_b + i_E R_e + V_{to} = 0$$

Since $\beta/\alpha_o = 1 + \beta$ and $i_C = \alpha_o i_E = \beta i_B$, then $i_E = (1 + \beta) i_B$

and

$$i_B = (V_{BB} - V_{to})/[R_e(1 + \beta) + R_b] \text{ or}$$

$$i_E = (V_{BB} - V_{to})/[R_e + R_b/(1 + \beta)]$$

Also,

$$i_C = \beta i_B = (V_{BB} - V_{to})/[R_e(1 + \beta)/(\beta) + R_b/(\beta)]$$

Kirchhoff's-Voltage-Law on Collector Side (the Load-Line Equation):

$$- V_{CC} + i_C R_c + i_E R_e + v_{EC} = 0 \quad \text{or} \quad v_{EC} = V_{CC} - i_C R_c - i_E R_e$$

If $\beta >> 1$, then $i_C \sim (V_{BB} - V_{to})/[R_e + R_b/(\beta)]$

If $R_e >> R_b/(\beta)$, then $i_C \sim (V_{BB} - V_{to})/(R_e)$

With no signal $v_S = 0$

$$V_o = i_C R_c = (R_c/R_e)(V_{BB} - V_{to})$$

With a signal v_S

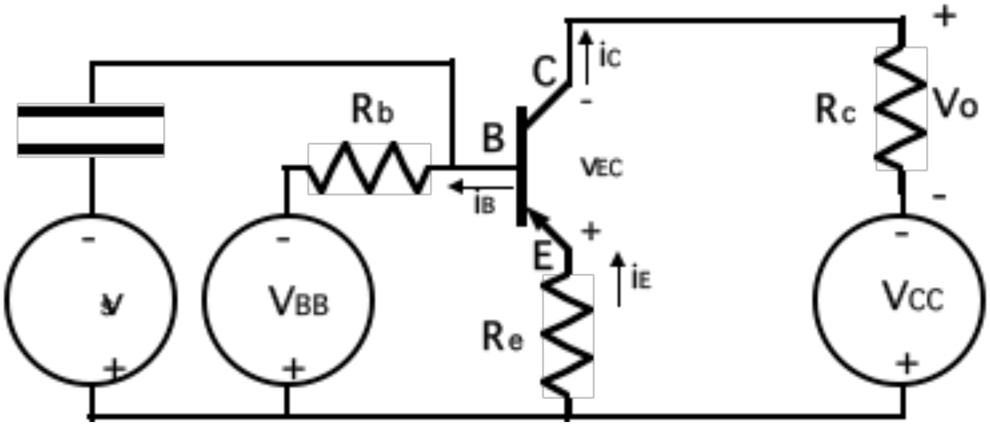
$$V_o = i_C R_c = (R_c/R_e)(V_{BB} - V_{to}) + (R_c/R_e)(v_S)$$

Note that for $v_S = 0$, this circuit serves as a constant current source, i.e. the current does not depend on the load resistance R_c.

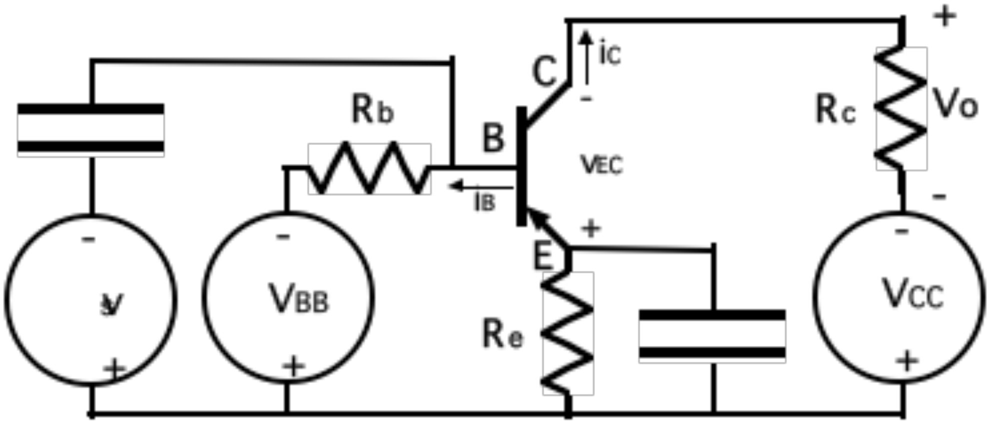
COMMON-EMITTER CIRCUITS WITH COUPLING CAPACITORS

Coupling Capacitor in pnp BJTs Common-Emitter Circuits

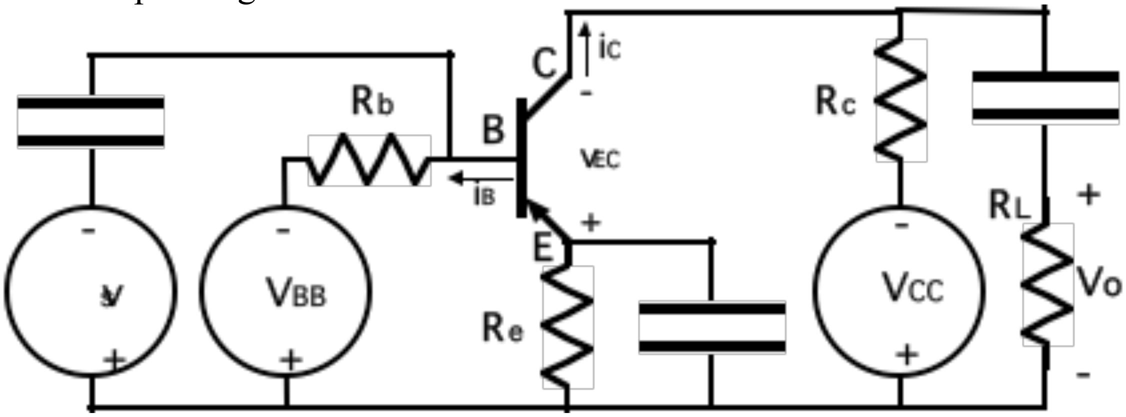
Separating Signal v_S and Biasing Source V_{BB}



Different AC and DC Load Lines



Separating the DC Current from the Load Resistance



CONSTANT CURRENT SOURCE WITH BJT

Constant Current Source (Common-Emitter) Circuit with an npn BJT

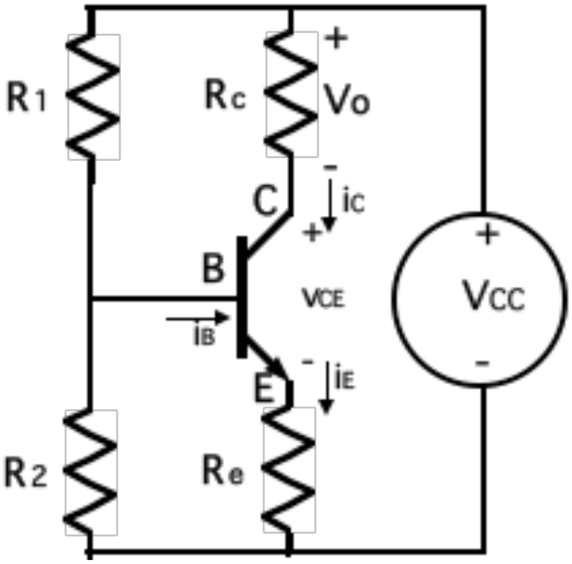
- Forward Bias of Base-Emitter Junctions v_{BE} > turn-on voltage
- Reverse Bias of Collector-Base Junctions $v_{BC} < 0$ or $v_{CB} > 0$

Consider the voltage source and the resistors R_1 and R_2 separately.

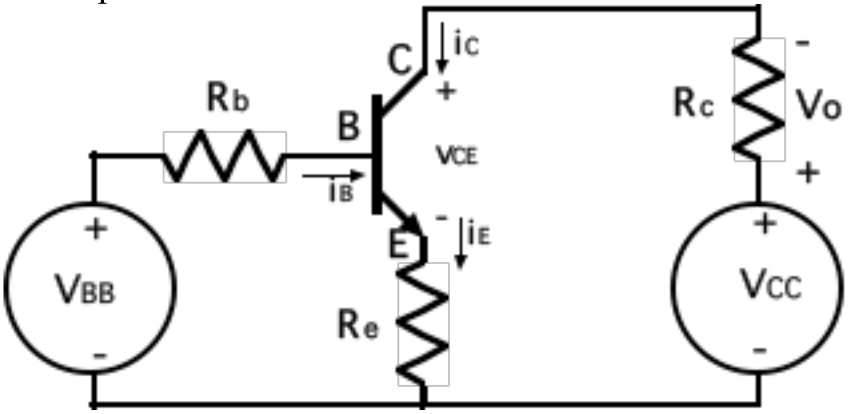
The Thevenin equivalent with respect to the Base node and the reference node has

$V_{BB} = V_{TH} = V_{CC} [R_2/(R_1 + R_2)]$

$R_b = R_{TH} = R_1||R_2 = [R_1R_2/(R_1 + R_2)]$



The equivalent circuit is



As before, the operating point (v_{CE}, i_C) is

$i_C = \beta i_B = (V_{BB} - V_{to})/[R_e(1 + \beta)/(\beta) + R_b/(\beta)]$ from KVL on base side

$v_{CE} = V_{CC} - i_CR_c - i_ER_e$ from KVL on collector side

If $\beta >> 1$, then $i_C \sim (V_{BB} - V_{to})/[R_e + R_b/(\beta)]$ (no dependence on R_c)

If $R_e >> R_b/(\beta)$, then $i_C \sim (V_{BB} - V_{to})/(R_e)$

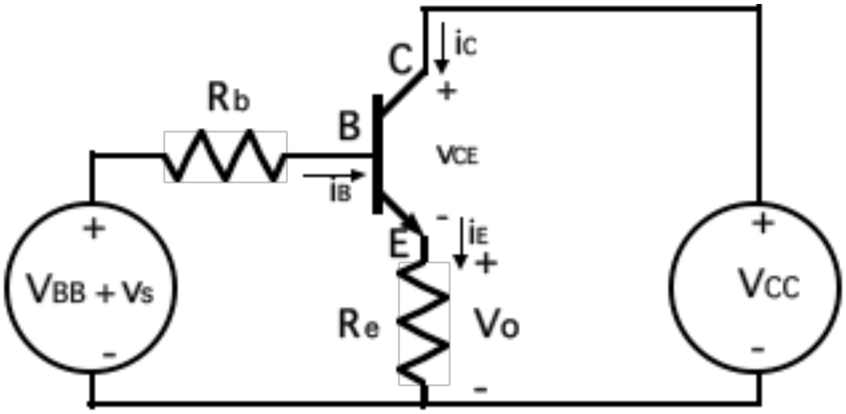
$V_o = i_CR_c = (R_c/R_e)(V_{BB} - V_{to})$

Only one voltage source is needed.

EMITTER-FOLLOWER BJT CIRCUIT AND ANALYSIS

Emitter-Follower Biasing Circuit with an npn BJT

- Forward Bias of Base-Emitter Junction v_{BE} > turn-on voltage
- Reverse Bias of Collector-Base Junction $v_{BC} < 0$ or $v_{CB} > 0$



Analysis for Operating Point (v_{CE},i_C) with $v_S = 0$.

Kirchhoff's-Voltage-Law on Base Side ($v_{BE} = V_{to}$):

$$- V_{BB} + i_B R_b + i_E R_e + V_{to} = 0$$

Since $\beta/\alpha_o = 1 + \beta$ and $i_C = \alpha_o i_E = \beta i_B$, then $i_E = (1 + \beta)i_B$
and

$$i_B = (V_{BB} - V_{to})/[R_e(1 + \beta) + R_b] \text{ or}$$

$$i_E = (V_{BB} - V_{to})/[R_e + R_b/(1 + \beta)]$$

Also,

$$i_C = \beta i_B = (V_{BB} - V_{to})/[R_e(1 + \beta)/(\beta) + R_b/(\beta)]$$

Kirchhoff's-Voltage-Law on Collector Side (the Load-Line Equation):

$$- V_{CC} + i_E R_e + v_{CE} = 0 \quad \text{or} \quad v_{CE} = V_{CC} - i_E R_e$$

If $R_e >> R_b/(1 + \beta)$, then $i_E \sim (V_{BB} - V_{to})/(R_e)$

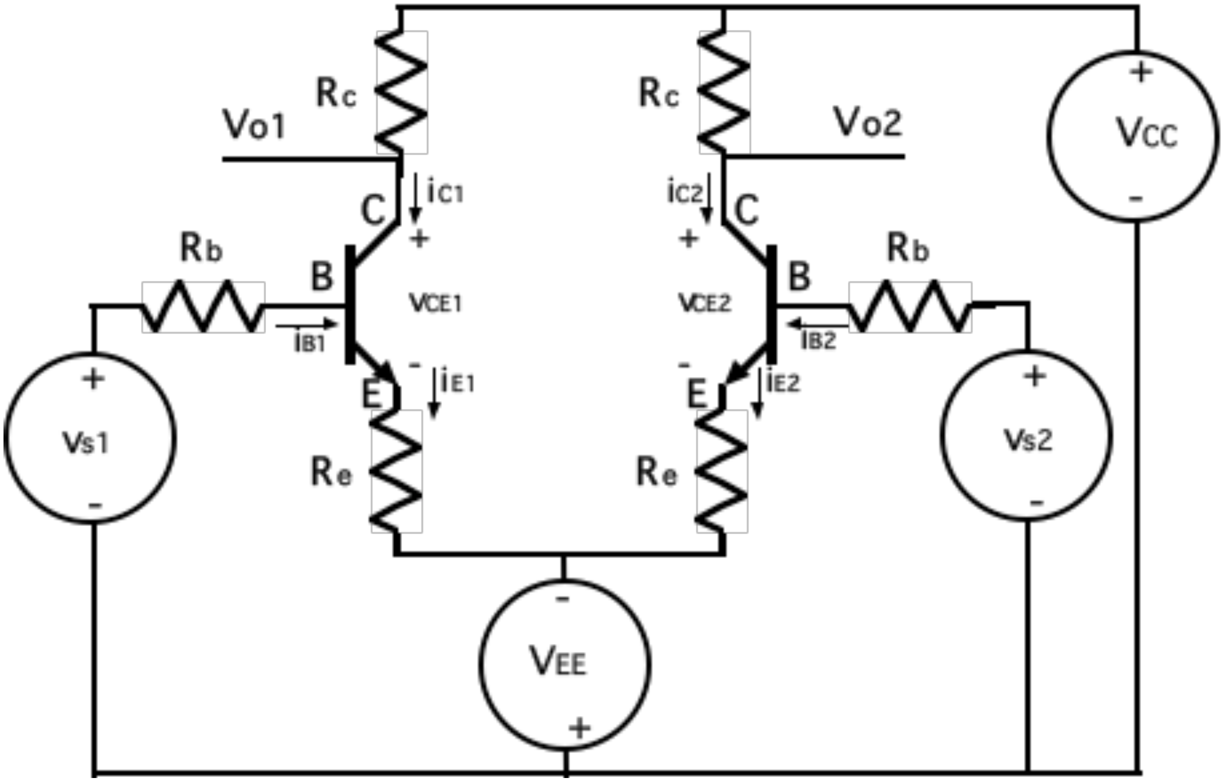
With no signal $v_S = 0$

$$V_o = i_E R_e = (V_{BB} - V_{to})$$

With a signal v_S

$$V_o = i_E R_e = (V_{BB} - V_{to}) + (v_S)$$

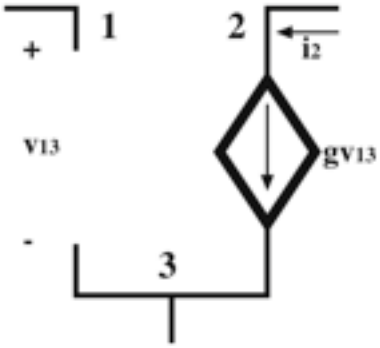
Differential Amplifier with npn BJTs



TRANSISTORS
FIELD EFFECT TRANSISTOR

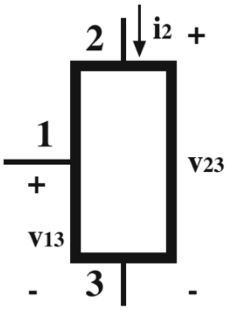
Transistor – a three-terminal device for which the voltage or current at one terminal controls the electrical behavior of the other terminals.

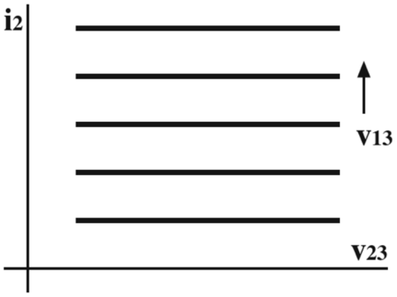
Field Effect Transistor (FET) – a three-terminal device for which a voltage related to one terminal controls the electrical behavior of the other terminals.



Voltage-Controlled (Dependent) Current Source

$i_2 = g\,v_{13}$





$i_2 = g\,v_{13}$

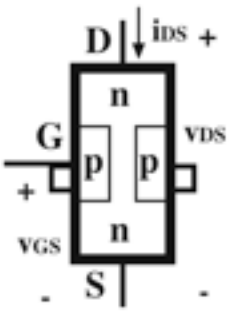
TRANSISTORS
FIELD EFFECT TRANSISTOR

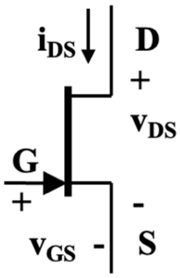
Junction Field Effect Transistor (JFET) – device formed by an n-type channel between two p-type materials or a p-type channel between two n-type materials.

Terminal Nomenclature

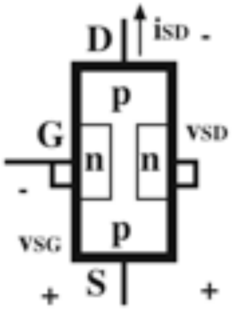
Gate (G), Drain (D), and Source (S)

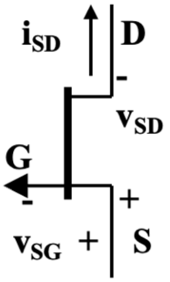
n-Channel JFET: Structure   Circuit Symbol



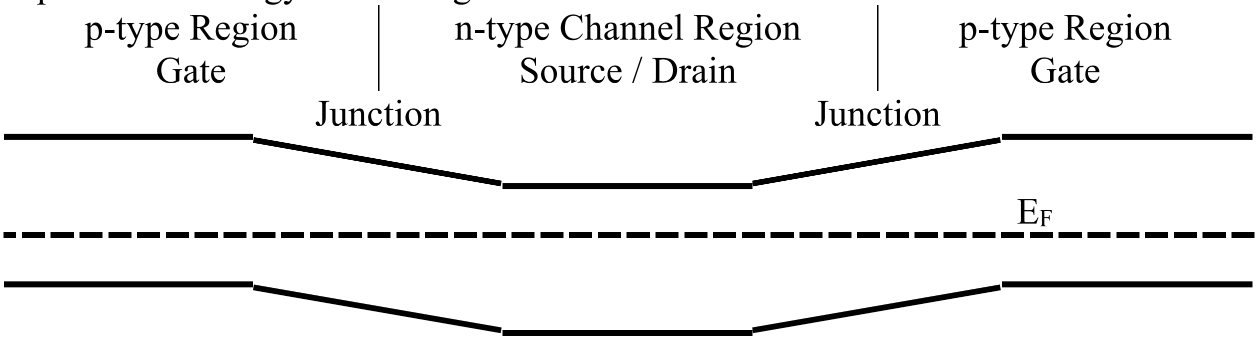


p-Channel JFET: Structure   Circuit Symbol





Equilibrium Energy Band Diagram for n-Channel Structure

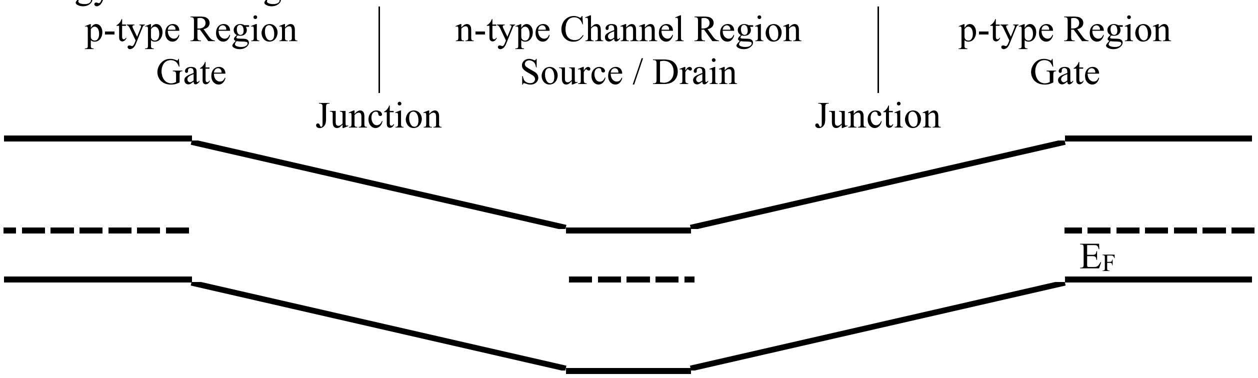


JFET OPERATING CONDITIONS

JFET Operating Conditions for n-Channel

- Gate-Channel Junction – Reverse Bias

Energy Band Diagram for Biased n-Channel Structure



Gate-Channel Junction under Reverse Bias

- Junction width broadens
- Drift current dominates (and is small)

Channel provides Drain-Source current path

- Current (mainly electrons) in the n-channel is dependent upon dimensions of undepleted channel
- Electrons travel from Source to Drain in the channel

Desired Operation

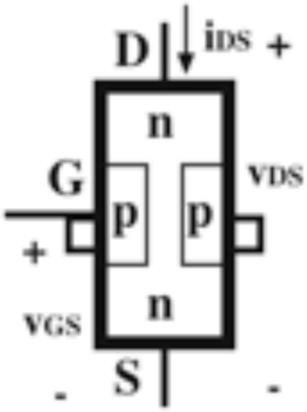
Current (mainly electrons) travels through the channel. The depletion region of the Gate-Channel junction constricts the channel as a function of Gate-Channel reverse bias and limits the current increase. As the depletion regions close the channel, further current increases go to zero and the channel is in saturation.

The design depends on the dimensions of the channel, the doping levels of the gate and channel, and breakdown characteristics of the gate-channel junction.

JFET PARAMETERS

JFET Current and Voltages – a summary of important current and voltages in an n-channel field-effect transistor is shown below. (Some secondary effects are omitted.)

- Drain-Source Voltage v_{DS} and Current i_{DS}
- Gate-Source Voltage v_{GS}
- Reverse-bias thermally-generated gate-channel current (neglected in further analysis) – Gate-Channel current ~ 0



Note that the Gate regions are electrically connected.

Pinch-off Voltage V_{po}: Gate-Channel Reverse-bias Voltage for which the opposite depletion regions merge

Saturation Current I_{DSS}: Drain-Source Current for saturation conditions (maximum current for $v_{GS} = 0$)

Note that the Gate-Channel Voltage varies as a function of position.

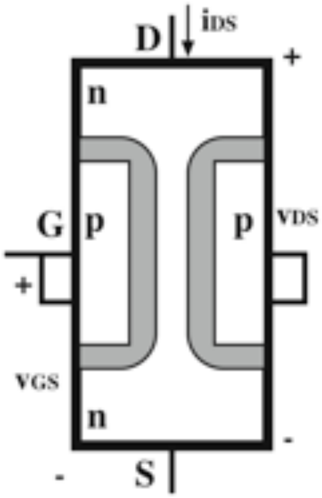
Design optimization

- Highly doped gate regions (p+): depletion regions extend primarily into the channel

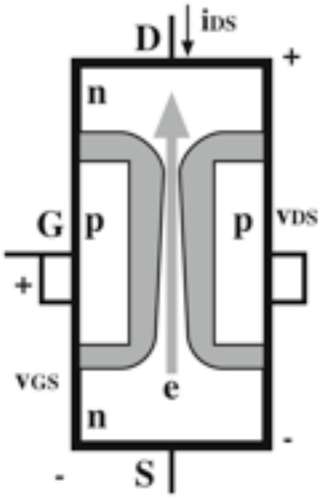
JFET CHARACTERISTIC

Physical Operation of the n-channel JFET

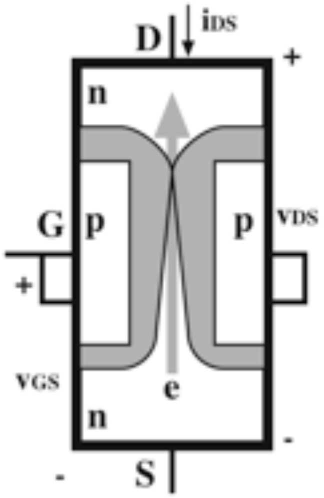
$v_{GS} = 0$ and $v_{DS} = 0$



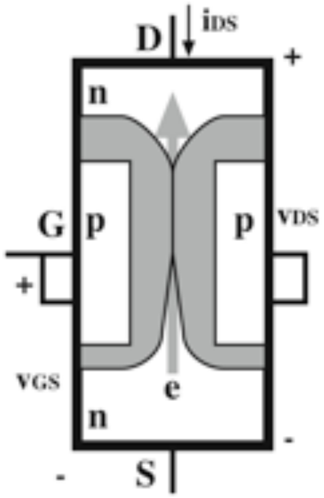
$v_{GS} = 0$ and $V_{po} > v_{DS} > 0$



$v_{GS} = 0$ and $v_{DS} = V_{po}$



$v_{GS} = 0$ and $v_{DS} > V_{po}$



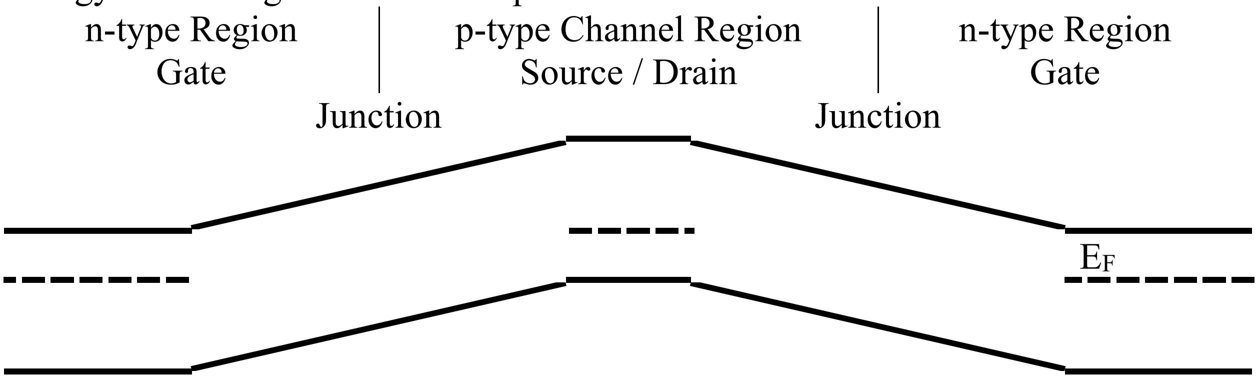
- Un-biased ($v_{GS} = 0$ and $v_{DS} = 0$): $i_{DS} = 0$
- Unsaturated Region with $v_{GS} = 0$ and $V_{po} > v_{DS} > 0$: i_{DS} increases, but at a decreasing rate due to channel constriction and
  $i_{DS} = I_{DSS}[2(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$
- Saturation Region with $v_{GS} = 0$ and $v_{DS} > V_{po} > 0$: $i_{DS} = I_{DSS}$ (current maintains the pinch-off condition with no further current increase)
- Influence of Gate-Channel bias ($-V_{po} < v_{GS} < 0$):
  Unsaturated: $i_{DS} = I_{DSS}[2(1 + v_{GS}/V_{po}) (v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$
  Saturation: $i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$

JFET OPERATING CONDITIONS

JFET Operating Conditions for p-Channel

- Gate-Channel Junction – Reverse Bias

Energy Band Diagram for Biased p-Channel Structure



Gate-Channel Junction under Reverse Bias

- Junction width broadens
- Drift current dominates (and is small)

Channel provides Drain-Source current path

- Current (mainly holes) in the p-channel is dependent upon dimensions of undepleted channel
- Holes travel from Source to Drain in the channel

Desired Operation

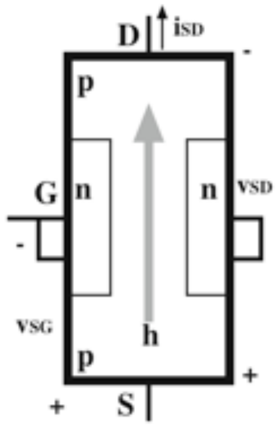
Current (mainly holes) travels through the channel. The depletion region of the Gate-Channel junction constricts the channel as a function of Gate-Channel reverse bias and limits the current increase. As the depletion regions close the channel, further current increases go to zero and the channel is in saturation.

The design depends on the dimensions of the channel, the doping levels of the gate and channel, and breakdown characteristics of the gate-channel junction.

JFET PARAMETERS

JFET Current and Voltages – a summary of important current and voltages in a p-channel field-effect transistor is shown below. (Some secondary effects are omitted.)

- Source-Drain Voltage v_{SD} and Current i_{SD}
- Source-Gate Voltage v_{SG}
- Reverse-bias thermally-generated gate-channel current (neglected in further analysis) – Gate-Channel current ~ 0



Note that the Gate regions are electrically connected.

Pinch-off Voltage V_{po}: Gate-Channel Reverse-bias Voltage for which the opposite depletion regions merge

Saturation Current I_{SDS}: Source-Drain Current for saturation conditions (maximum current for $v_{SG} = 0$)

Note that the Gate-Channel Voltage varies as a function of position.

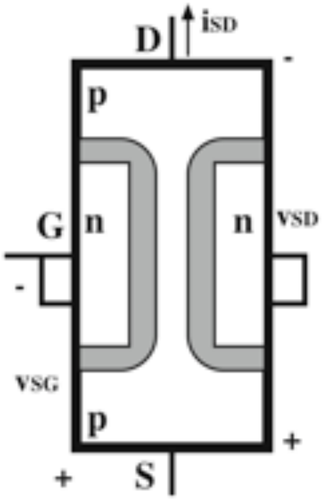
Design optimization

- Highly doped gate regions (n+): depletion regions extend primarily into the channel

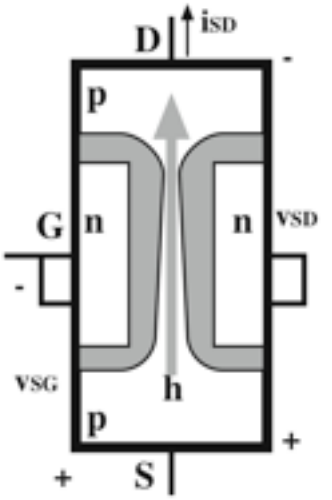
JFET CHARACTERISTIC

Physical Operation of the p-channel JFET

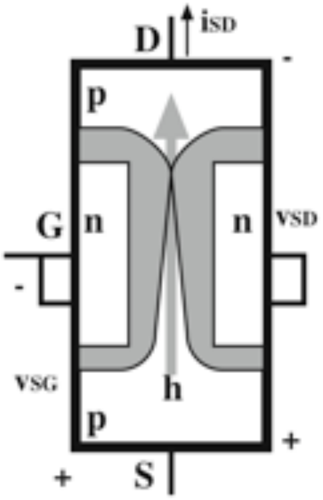
$v_{SG} = 0$ and $v_{SD} = 0$



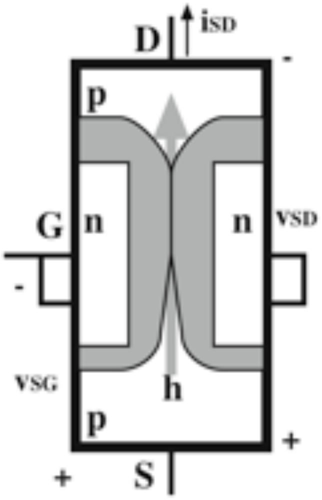
$v_{SG} = 0$ and $V_{po} > v_{SD} > 0$



$v_{SG} = 0$ and $v_{SD} = V_{po}$



$v_{SG} = 0$ and $v_{SD} > V_{po}$



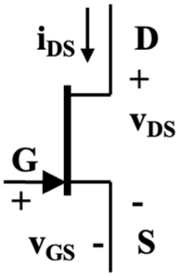
- Un-biased ($v_{SG} = 0$ and $v_{SD} = 0$): $i_{SD} = 0$
- Unsaturated Region with $v_{SG} = 0$ and $V_{po} > v_{SD} > 0$: i_{SD} increases, but at a decreasing rate due to channel constriction and
  $i_{SD} = I_{SDS}[2(v_{SD}/V_{po}) - (v_{SD}/V_{po})^2]$
- Saturation Region with $v_{SG} = 0$ and $v_{SD} > V_{po} > 0$: $i_{SD} = I_{SDS}$ (current maintains the pinch-off condition with no further current increase)
- Influence of Gate-Channel bias ($-V_{po} < v_{SG} < 0$):
  Unsaturated: $i_{SD} = I_{SDS}[2(1 + v_{SG}/V_{po})(v_{SD}/V_{po}) - (v_{SD}/V_{po})^2]$
  Saturation: $i_{SD} = I_{SDS}(1 + v_{SG}/V_{po})^2$

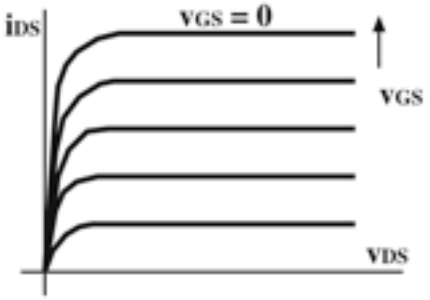
CONDITIONS FOR JFET SATURATION

JFET Saturation Conditions for n-Channel

- Gate-Drain Junction at Reverse-Bias pinch-off voltage V_{po}

n-Channel JFET





Kirchhoff's-Voltage-Law for n-channel JFET:

$- v_{GS} - v_{DG} + v_{DS} = 0$ or $v_{DG} = v_{DS} - v_{GS}$

General pinch-off condition including influence of Gate-Channel bias:

$$v_{DG} = v_{DS} - v_{GS} \geq V_{po}$$

- Unsaturated Region of Operation: $V_{po} > v_{DS} - v_{GS} > 0$
  $$i_{DS} = I_{DSS}[2(1 + v_{GS}/V_{po})\,(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$$
- Saturation Region of Operation: $v_{DS} - v_{GS} \geq V_{po} > 0$
  $$i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2 \quad \text{for } -V_{po} < v_{GS} < 0$$

The IV characteristic is continuous at the threshold of saturation.

Let $v_{DS} - v_{GS} = V_{po}$ or $v_{DS} = V_{po} + v_{GS}$

$$i_{DS} = I_{DSS}[2(1 + v_{GS}/V_{po})\,(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$$
$$i_{DS} = I_{DSS}\{2(1 + v_{GS}/V_{po})\,[(V_{po} + v_{GS})/V_{po}] - [(V_{po} + v_{GS})/V_{po})]^2\}$$
$$i_{DS} = I_{DSS}[(2 + 2v_{GS}/V_{po})\,(1 + v_{GS}/V_{po}) - (1 + v_{GS}/V_{po})^2]$$
$$i_{DS} = I_{DSS}[2 + 4v_{GS}/V_{po} + 2(v_{GS}/V_{po})^2 - 1 - 2\,v_{GS}/V_{po} - (v_{GS}/V_{po})^2]$$
$$i_{DS} = I_{DSS}[1 + 2v_{GS}/V_{po} + (v_{GS}/V_{po})^2]$$
$$i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$$

General pinch-off condition for p-channel JFET

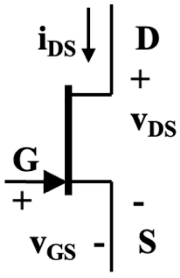
$$v_{GD} = v_{SD} - v_{SG} \geq V_{po}$$

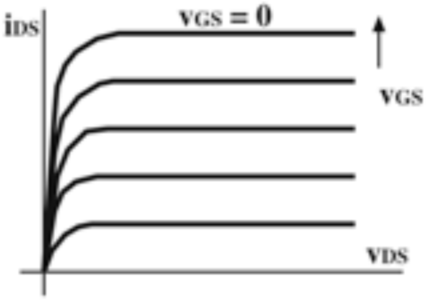
- Unsaturated Region of Operation: $V_{po} > v_{SD} - v_{SG} > 0$
  $$i_{SD} = I_{SDS}[2(1 + v_{SG}/V_{po})\,(v_{SD}/V_{po}) - (v_{SD}/V_{po})^2]$$
- Saturation Region of Operation: $v_{SD} - v_{SG} \geq V_{po} > 0$
  $$i_{SD} = I_{SDS}(1 + v_{SG}/V_{po})^2 \text{ for } -V_{po} < v_{SG} < 0$$

SUMMARY OF JFET BEHAVIOR

The junction field effect transistor with pinch-off voltage V_{po}

n-Channel JFET



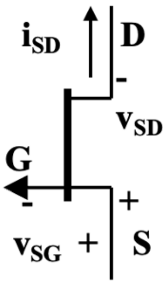


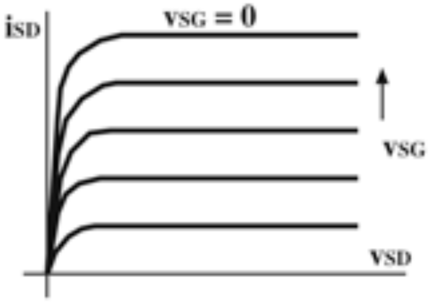
n-Channel JFET Operating Conditions

- Reverse Bias of Gate-Channel Junction: $v_{DS} > 0$ and $-V_{po} < v_{GS} < 0$

$i_{DS} = I_{DSS}[2(1 + v_{GS}/V_{po})(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$ and $i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$.

p-Channel JFET





p-Channel JFET Operating Conditions

- Reverse Bias of Gate-Channel Junction: $v_{SD} > 0$ and $-V_{po} < v_{SG} < 0$

$i_{SD} = I_{SDS}[2(1 + v_{SG}/V_{po})(v_{SD}/V_{po}) - (v_{SD}/V_{po})^2]$ and $i_{SD} = I_{SDS}(1 + v_{SG}/V_{po})^2$.

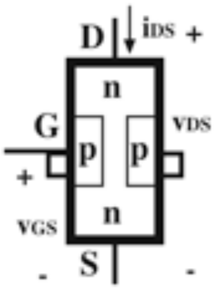
Regions in the JFET IV Characteristic

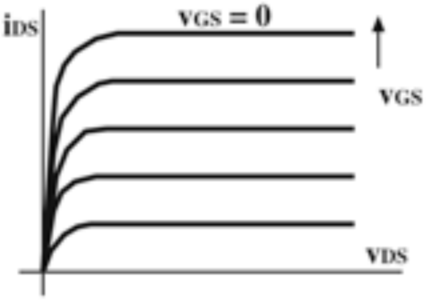
- Unsaturated Region – the channel is below pinch-off and the current i_{DS} varies strongly with v_{DS} or v_{SD}.
- Saturation Region – the channel is above pinch-off and the current i_{DS} varies strongly with v_{GS} or v_{SG}.
- Breakdown (not shown) – the limit for large values of v_{DS} (n-channel) or v_{SD} (p-channel) when breakdown occurs in the gate-channel junction

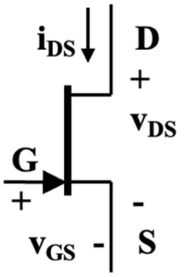
Other secondary effects may be considered for more accurate representations, but these effects are beyond the scope of this class.

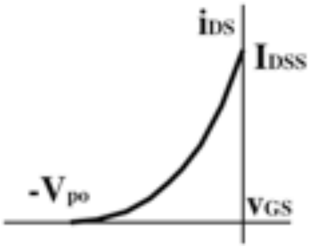
COMPARISON OF FET STRUCTURES

Junction Field Effect Transistor (JFET): n-Channel

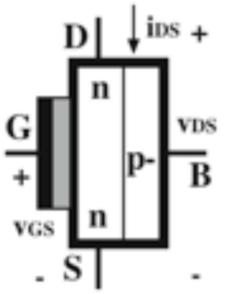


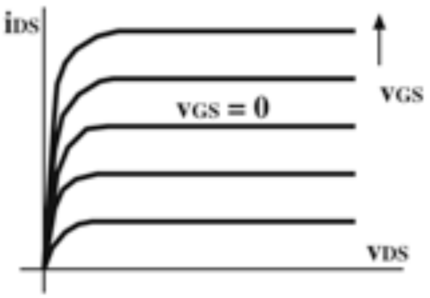


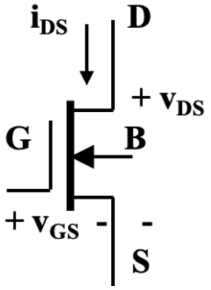


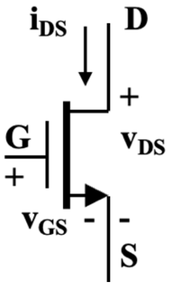


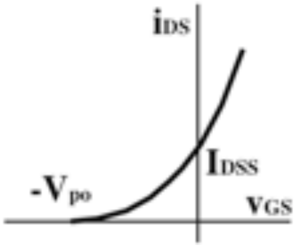
Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET):
Depletion-Mode n-Channel







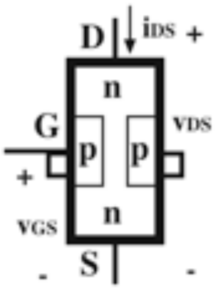


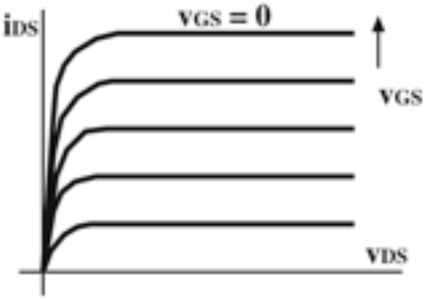


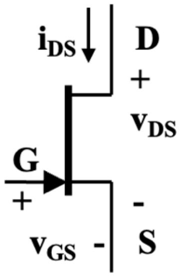
Base Separate   Base Connected to Source

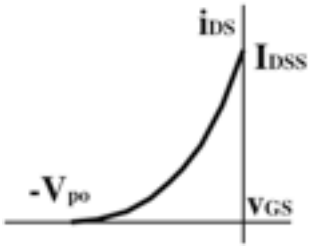
COMPARISON OF FET STRUCTURES

Junction Field Effect Transistor (JFET): n-Channel

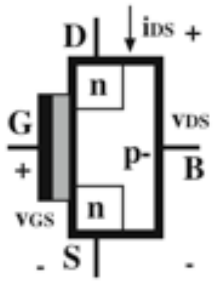


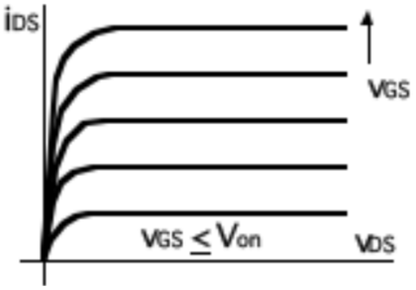


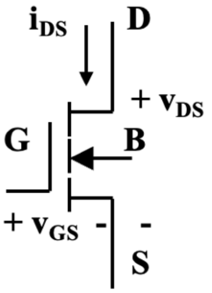




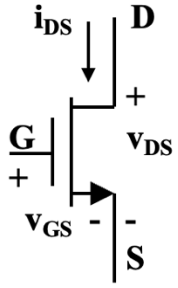
Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET):
Enhancement-Mode n-Channel



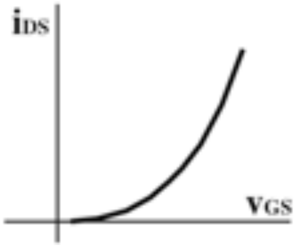




Base Separate

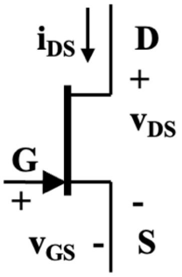


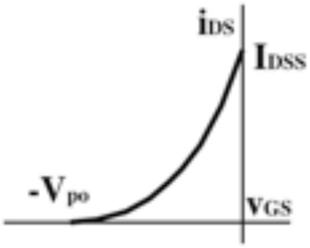
Base Connected to Source

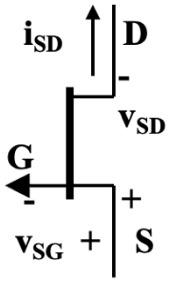


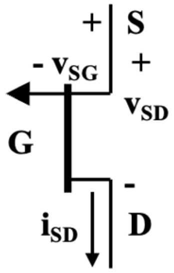
SUMMARY OF FET TYPES

Junction Field Effect Transistor (JFET): n-Channel and p-channel
n-Channel JFET Equations
$i_{DS} = I_{DSS}[2(1 + v_{GS}/V_{po})(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$ & $i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$.
The JFET turns on when $0 > v_{GS/SG} > -V_{po}$.

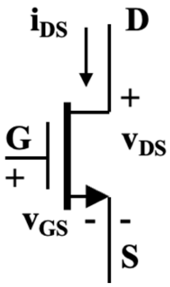


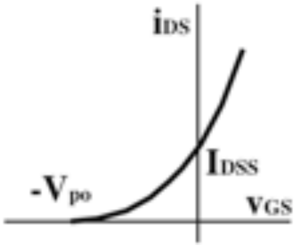


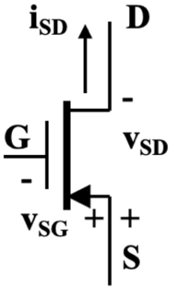


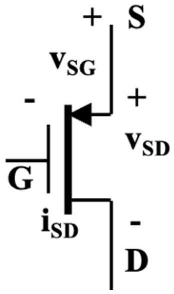


Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET):
Depletion-Mode n-Channel and p-Channel (Base connected to Source)
Depletion-Mode n-Channel MOSFET Equations
$i_{DS} = I_{DSS}[2(1 + v_{GS}/V_{po})(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$ & $i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$.
The Depletion-Mode MOSFET turns on when $v_{GS/SG} > -V_{po}$.

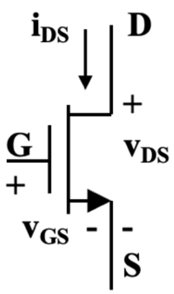


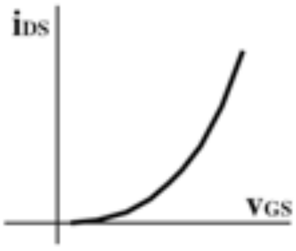


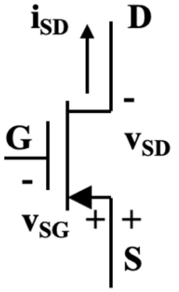


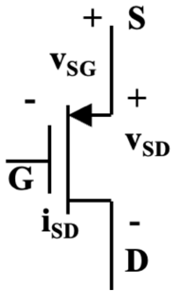


Enhancement-Mode n-Channel and p-Channel (Base connected to Source)
Enhancement-Mode n-Channel MOSFET Equations
$i_{DS} = KV_{on}^2\{2[(v_{GS}/V_{on}) - 1](v_{DS}/V_{on}) - (v_{DS}/V_{on})^2\}$ &
$i_{DS} = KV_{on}^2[(v_{GS}/V_{on}) - 1]^2$.
The Enhancement-Mode MOSFET turns on when $v_{GS/SG} > V_{on} > 0$.





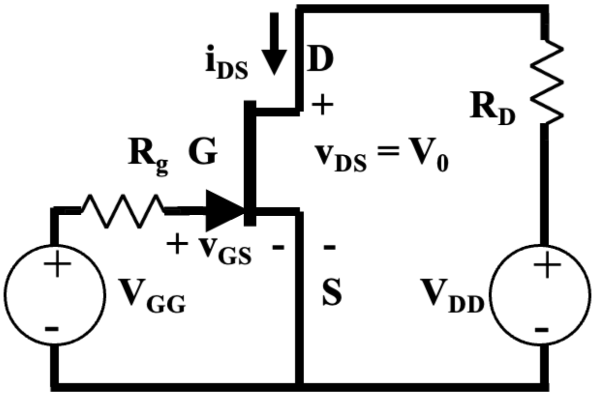




COMMON-SOURCE JFET CIRCUIT AND ANALYSIS

Common-Source Biasing Circuit with an n-channel JFET

- Reverse Bias of Gate-Channel $-V_{po} < v_{GS} < 0$ and $v_{DS} > 0$
- "On" for $i_{DS} > 0$ and "Off" for $i_{DS} = 0$



Analysis for Operating Point (v_{DS}, i_{DS}).

The Gate Voltage determines the Drain-Source Current ($V_{GG} = v_{GS}$).

For $-V_{po} < v_{GS} < 0$, then $i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$.

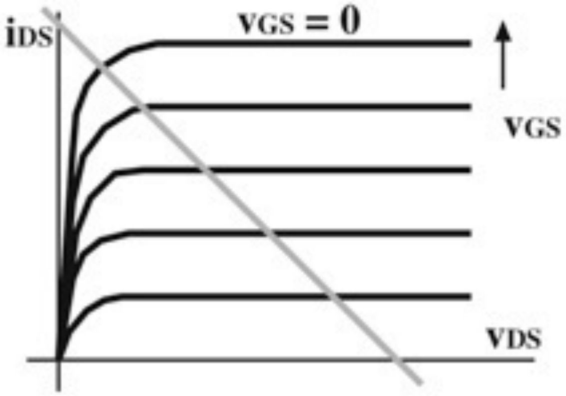
Kirchhoff's-Voltage-Law on Drain Side (the Load-Line Equation):

$- V_{DD} + i_{DS} R_d + v_{DS} = 0$ or $v_{DS} = V_{DD} – i_{DS}R_d$

For operation in the saturation region, the Output Voltage is

$V_O = v_{DS} = V_{DD} – i_{DS}R_d = V_{DD} – [I_{DSS}(1 + v_{GS}/V_{po})^2]R_d$

Graphical Analysis



Load-Line

$-V_{DD} + i_{DS} R_d + v_{DS} = 0$

Intercepts

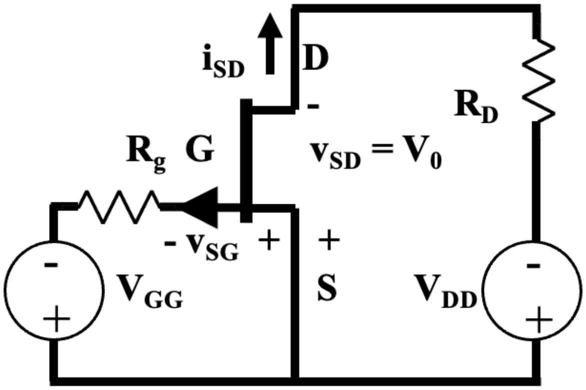
$v_{DS} = V_{DD}$

$i_{DS} = V_{DD}/R_d$

COMMON-SOURCE JFET CIRCUIT AND ANALYSIS

Common-Source Biasing Circuit with a p-channel JFET

- Reverse Bias of Gate-Channel $-V_{po} < v_{SG} < 0$ and $v_{SD} > 0$
- "On" for $i_{SD} > 0$ and "Off" for $i_{SD} = 0$



Analysis for Operating Point (v_{SD}, i_{SD}).

The Gate Voltage determines the Drain-Source Current ($V_{GG} = v_{SG}$).

For $-V_{po} < v_{SG} < 0$, then $i_{SD} = I_{SDS}(1 + v_{SG}/V_{po})^2$.

Kirchhoff's-Voltage-Law on Drain Side (the Load-Line Equation):

$- V_{DD} + i_{SD} R_d + v_{SD} = 0$ or $v_{SD} = V_{DD} – i_{SD}R_d$

For operation in the saturation region, the Output Voltage is

$V_O = v_{SD} = V_{DD} – i_{SD}R_d = V_{DD} – [I_{SDS}(1 + v_{SG}/V_{po})^2]R_d$

Graphical Analysis

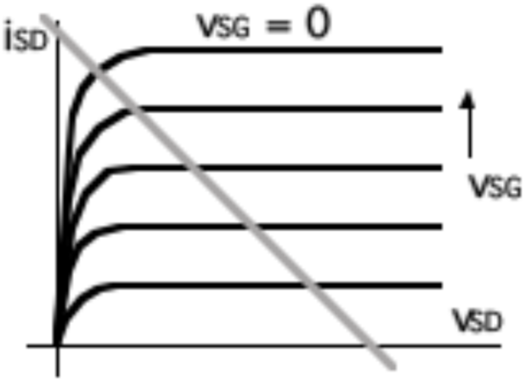
Load-Line

$-V_{DD} + i_{SD} R_d + v_{SD} = 0$

Intercepts

$v_{SD} = V_{DD}$

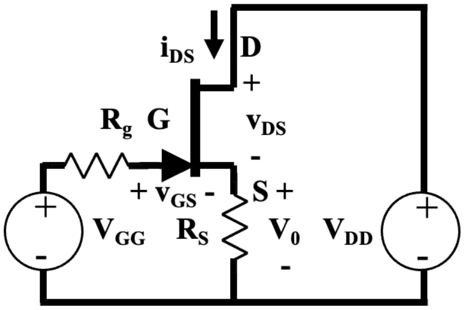
$i_{SD} = V_{DD}/R_d$



SOURCE-FOLLOWER JFET CIRCUIT AND ANALYSIS

Source-Follower Biasing Circuit with an n-channel JFET

- Reverse Bias of Gate-Channel $-V_{po} < v_{GS} < 0$ and $v_{DS} > 0$
- "On" for $i_{DS} > 0$ and "Off" for $i_{DS} = 0$



Analysis for Operating Point (v_{DS}, i_{DS}).

Kirchhoff's-Voltage-Law on Gate-Source Side:

$- V_{GG} + i_{DS} R_s + v_{GS} = 0$ or $v_{GS} = V_{GG} - i_{DS}R_s$

and for operation in the saturation region

$-V_{po} < v_{GS} = (V_{GG} - i_{DS}R_s) < 0$ and $i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$.

Kirchhoff's-Voltage-Law on Drain Side (the Load-Line Equation):

$- V_{DD} + i_{DS} R_s + v_{DS} = 0$ or $v_{DS} = V_{DD} - i_{DS}R_s$

For operation in the saturation region, the Output Voltage is

$V_O = i_{DS} R_s = I_{DSS}R_s(1 + v_{GS}/V_{po})^2 = I_{DSS}R_s[1 + (V_{GG} - i_{DS}R_s)/V_{po}]^2$.

Graphical Analysis

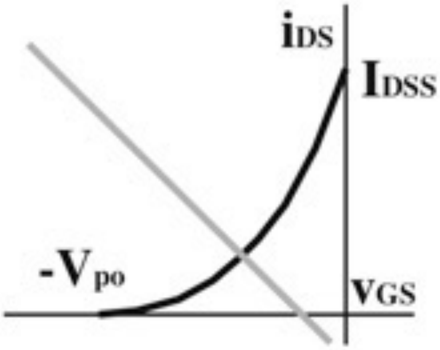
Gate-Source Equation

$-V_{GG} + i_{DS} R_s + v_{GS} = 0$

Intercepts

$V_{GS} = V_{GG}$

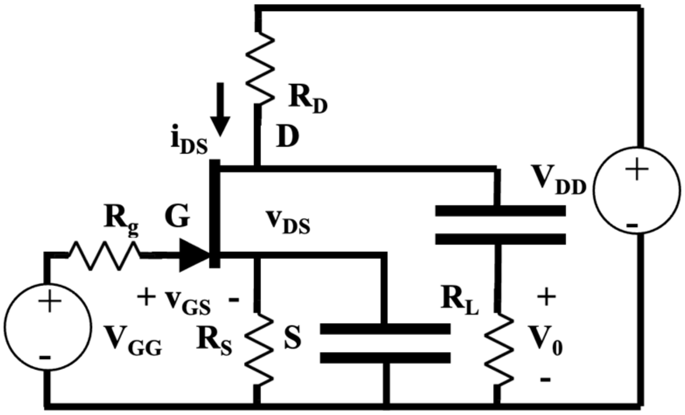
$i_{DS} = V_{GG}/R_s$



OTHER COMMON-SOURCE CIRCUITS

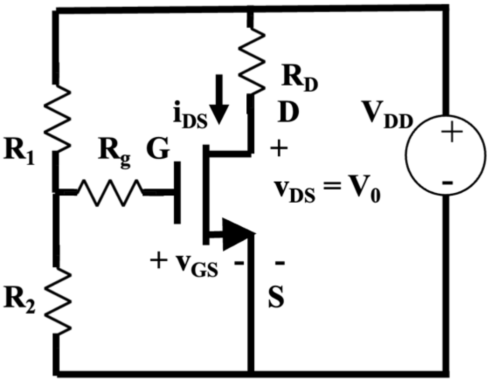
Coupling Capacitors in n-Channel JFET Common-Emitter Circuit

Different AC and DC Load Lines



Single-Source in n-Channel Enhancement-Mode MOSFET Circuit

Thevenin Equivalent Circuit for Input Voltage



$$V_{GG} = V_{TH} = V_{DD} [R_2/(R_1 + R_2)]$$

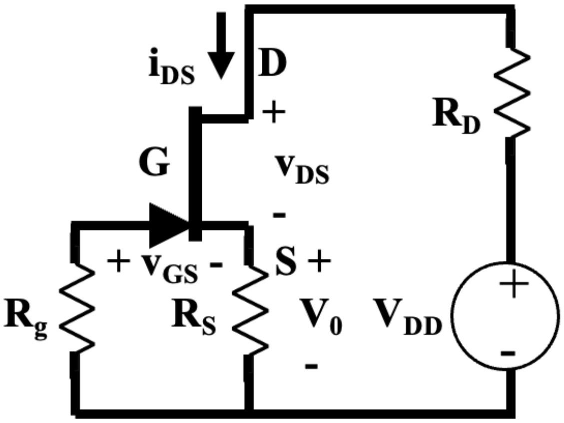
$$R_{TH} = R_1||R_2 = [R_1R_2/(R_1 + R_2)]$$

SELF-BIASING JFET CIRCUIT

Self-Biasing Circuit with an n-channel JFET

- Reverse Bias of Gate-Channel $-V_{po} < v_{GS} < 0$ and $v_{DS} > 0$

Analysis for Operating Point
(v_{DS}, i_{DS}).



Kirchhoff's-Voltage-Law for Gate-Source gives ($i_G = 0$).

$v_{GS} = -i_{DS} R_s$

For $-V_{po} < v_{GS} < 0$, then

$i_{DS} = I_{DSS}(1 + v_{GS}/V_{po})^2$

$i_{DS} = I_{DSS}[1 + (-i_{DS} R_s)/V_{po}]^2$.

Kirchhoff's-Voltage-Law on Drain Side (the Load-Line Equation):

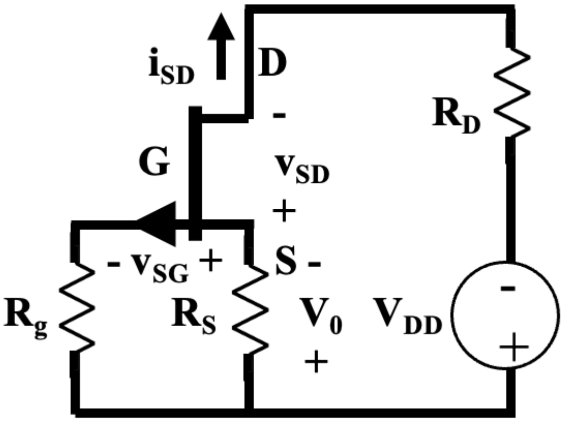
$-V_{DD} + i_{DS} (R_d + R_s) + v_{DS} = 0$

or $v_{DS} = V_{DD} - i_{DS}(R_d + R_s)$

Self-Biasing Circuit with a p-channel JFET

- Reverse Bias of Gate-Channel $-V_{po} < v_{SG} < 0$ and $v_{SD} > 0$

Analysis for Operating Point
(v_{SD}, i_{SD}).



Kirchhoff's-Voltage-Law for Gate-Source gives ($i_G = 0$).

$v_{SG} = -i_{SD} R_s$

For $-V_{po} < v_{SG} < 0$, then

$i_{SD} = I_{SDS}(1 + v_{SG}/V_{po})^2$

$i_{SD} = I_{SDS}[1 + (-i_{SD} R_s)/V_{po}]^2$.

Kirchhoff's-Voltage-Law on Drain Side (the Load-Line Equation):

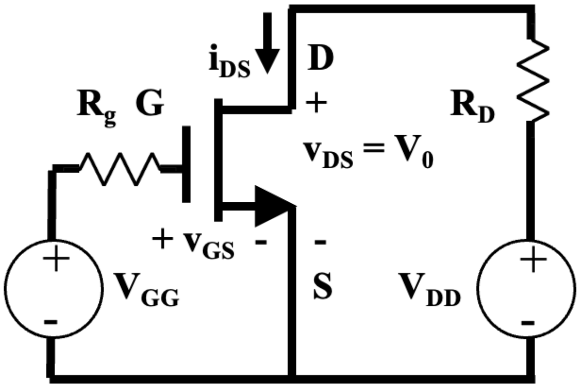
$-V_{DD} + i_{SD} (R_d + R_s) + v_{SD} = 0$

or $v_{SD} = V_{DD} - i_{SD}(R_d + R_s)$

ENHANCEMENT-MODE MOSFET CIRCUIT

Passive Drain Load on an Enhancement-Mode n-channel MOSFET

- Reverse Bias of Gate-Channel $0 < V_{on} < v_{GS}$ and $v_{DS} > 0$
- "On" for $i_{DS} > 0$ ($V_{on} < v_{GS}$) and "Off" for $i_{DS} = 0$ ($V_{on} > v_{GS}$)
- $v_{GS} = V_{GG} = V_i$ (since $i_G = 0$)



Analysis for Operating Point (v_{DS}, i_{DS}).

The Gate Voltage determines the Drain-Source Current ($v_{GS} = V_{GG} = V_i$).
For $0 < V_{on} < v_{GS} = V_i$, then $i_{DS} = KV_{on}^2(v_{GS}/V_{on} - 1)^2$.

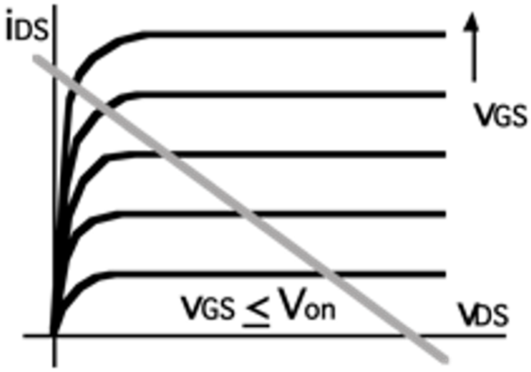
Kirchhoff's-Voltage-Law on Drain Side (the Load-Line Equation):
$- V_{DD} + i_{DS} R_d + v_{DS} = 0$ or $v_{DS} = V_{DD} - i_{DS}R_d$

Note the inverter behavior. A low input voltage produces a high output voltage and a high input produces a low output.

Graphical Analysis

Load-Line
$-V_{DD} + i_{DS} R_d + v_{DS} = 0$

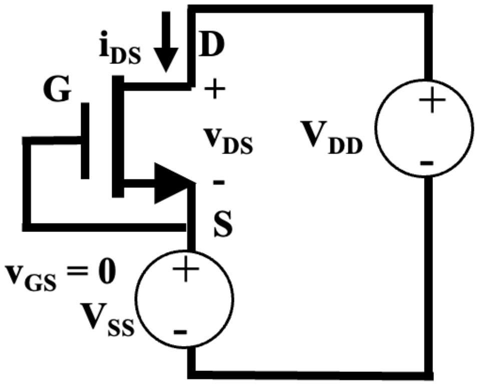
Intercepts
$v_{DS} = V_{DD}$
$i_{DS} = V_{DD}/R_d$



DEPLETION-MODE MOSFET CIRCUIT

Depletion-Mode n-channel MOSFET as an Active Load

- Reverse Bias of Gate-Channel $v_{DS} > 0$
- Gate connected to the Source $v_{GS} = 0$



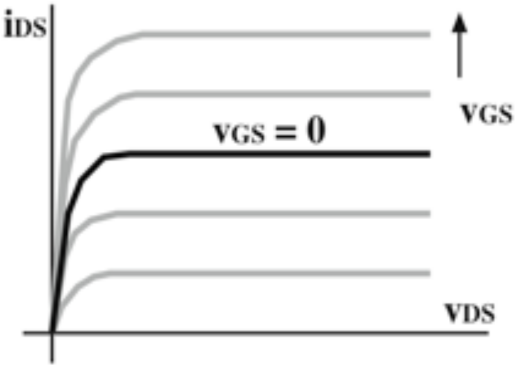
Analysis for Operating Point (v_{DS}, i_{DS}).

The Gate Voltage determines the Drain-Source Current ($v_{GS} = 0$).

$i_{DS} = I_{DSS}[2(1 + 0)(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$ & $i_{DS} = I_{DSS}(1 + 0)^2$.

Kirchhoff's-Voltage-Law on Drain Side (the Load-Line Equation):

$- V_{DD} + V_{SS} + v_{DS} = 0$ or $v_{DS} = V_{DD} - V_{SS}$



Graphical Analysis

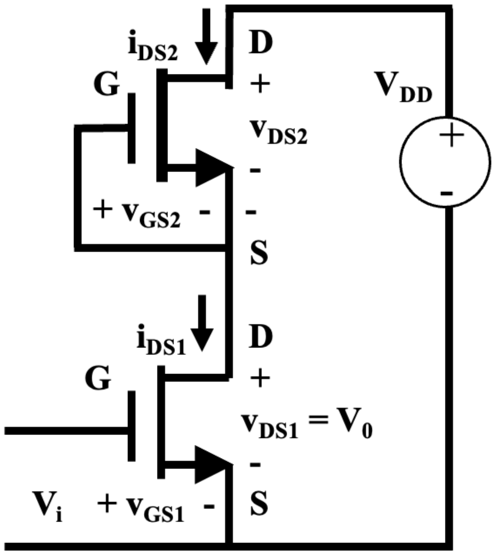
For $v_{DS} = V_{DD} - V_{SS} > V_{po}$
Then $i_{DS} = I_{DSS}$

For $v_{DS} = V_{DD} - V_{SS} < V_{po}$
Then $i_{DS} =$
$I_{DSS}[2(v_{DS}/V_{po}) - (v_{DS}/V_{po})^2]$

ENHANCEMENT-MODE MOSFET INVERTER CIRCUIT

Active Drain Load on an Enhancement-Mode n-channel MOSFET

- Enhancement-Mode MOSFET with Input $V_i = v_{GS1}$
- Depletion-Mode MOSFET with $v_{GS2} = 0$



Analysis for V_o vs. V_i

Kirchhoff's-Voltage-Law (the Load-Line Equation):

$- V_{DD} + v_{DS2} + v_{DS1} = 0$ or $v_{DS1} = V_{DD} - v_{DS2}$

Extremes

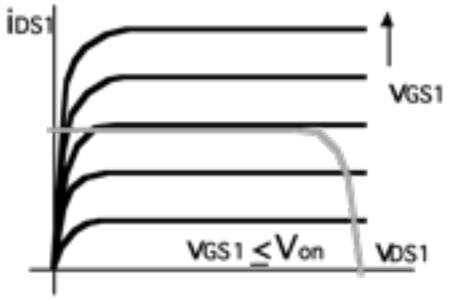
Input Low $V_i = v_{GS1} \leq V_{on}$, (MOSFET 1 "Off" and MOSFET 2 "Off")

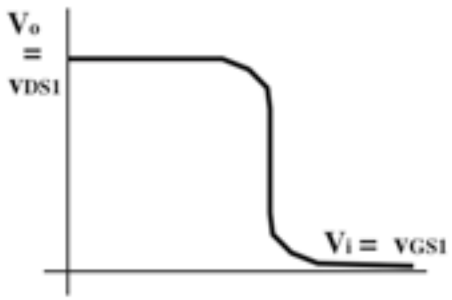
$i_{DS1} = i_{DS2} = 0$; then $v_{DS2} = 0$ and (LL) $v_{DS1} = V_{DD}$

Input High $V_i = v_{GS1} >> V_{on}$ (such that $v_{DS2} > V_{po}$),

(MOSFET 1Unsaturated and MOSFET 2 Saturated)

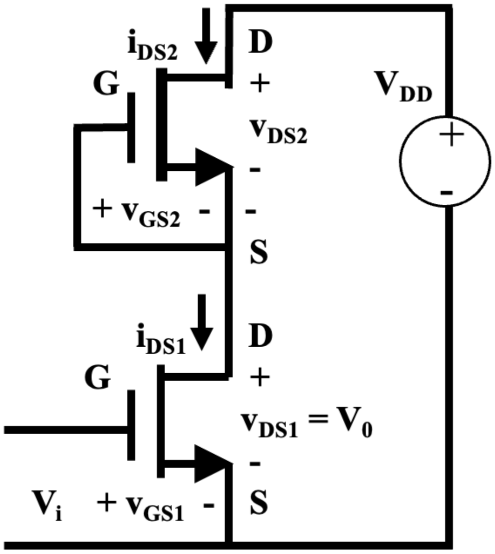
$i_{DS1} = i_{DS2} = I_{DSS2}$; then (LL) v_{DS1} approaches 0 V





ENHANCEMENT-MODE MOSFET INVERTER CIRCUIT

Active Drain Load on an Enhancement-Mode n-channel MOSFET



Progression

For $V_i = v_{GS1} \le V_{on}$, $i_{DS1} = i_{DS2} = 0$; then $v_{DS2} = 0$ and (LL) $v_{DS1} = V_{DD}$
(MOSFET 1 “Off” and MOSFET 2 “Off”)
Low Input and High Output

For $V_i = v_{GS1} = V_{on}^{+}$ and $v_{DS2} < V_{po}$, $i_{DS1} = i_{DS2} < I_{DSS2}$;
(MOSFET 1 Saturated and MOSFET 2 Unsaturated)

For $V_i = v_{GS1} > V_{on}^{+}$ and $v_{DS2} \ge V_{po}$, $i_{DS1} = i_{DS2} = I_{DSS2}$;
(MOSFET 1 Saturated and MOSFET 2 Saturated)

For $V_i = v_{GS1} >> V_{on}$ and $v_{DS2} \sim V_{DD}$, $i_{DS1} = i_{DS2} = I_{DSS2}$;
(MOSFET 1Unsaturated and MOSFET 2 Saturated)
High Input and Low Output